

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2, 4, 6-25, 49-64, and 66-70 (Canceled)

1 71. (New) An integrated circuit package comprising:
2 a silicon die having a first thickness;
3 a substrate having a first side and a second side;
4 a transition medium disposed between the silicon die and the first side of the
5 substrate; and
6 a mold cap which encapsulates the silicon die and the transition medium, wherein
7 the transition medium and the mold cap expand and contract at approximately the same rate in
8 response to temperature changes so as to reduce thermal stress on the silicon die during thermal
9 cycling.

1 72. (New) The integrated circuit package of claim 71, wherein the
2 transition medium and the mold cap have approximately equal coefficients of thermal expansion.

1 73. (New) The integrated circuit package of claim 71, wherein the
2 mold cap and transition medium have coefficients of thermal expansion between approximately
3 $7 \times 10^{-6}/^{\circ}\text{C}$ and $15 \times 10^{-6}/^{\circ}\text{C}$.

1 74. (New) The integrated circuit package of claim 71, wherein the
2 transition medium has a second thickness, and the first thickness of the silicon die is less than the
3 second thickness of the transition medium.

1 75. (New) The integrated circuit package of claim 71, wherein a first
2 edge of the transition medium is coincident with a first edge of the silicon die, and a second edge
3 of the transition medium is coincident with a second edge of the silicon die.

1 76. (New) The integrated circuit package of claim 71 wherein a
2 thickness of the substrate and a thickness of the mold cap define a package thickness, wherein
3 the silicon die is disposed at a location approximately equally spaced from the bottom of the
4 substrate and the top of the mold cap.

1 77. (New) The integrated circuit package of claim 76 wherein the
2 mold cap has a coefficient of thermal expansion similar to a coefficient of thermal expansion of
3 the transition medium such that the die remains relatively motionless within the integrated circuit
4 package during thermal cycling.

1 78. (New) The integrated circuit package of claim 71 wherein the
2 silicon die is coupled to the transition medium through an adhesive.

1 79. (New) The integrated circuit package of claim 78, wherein a
2 coefficient of thermal expansion for the adhesive is approximately $58 \times 10^{-6}/^{\circ}\text{C}$.

1 80. (New) The integrated circuit package of claim 71 wherein the
2 substrate is a tape carrier having a dielectric layer and a conductive layer.

1 81. (New) The integrated circuit package of claim 80 comprising
2 solder balls mounted to the second side of the substrate, the solder balls electrically contacting an
3 etched circuit in a conductive layer of the tape carrier and adapted to electrically connect the
4 integrated circuit package to a printed circuit board.

1 82. (New) The integrated circuit package of claim 81, wherein the
2 transition medium and the mold cap have coefficients of thermal expansion less than a
3 coefficient of thermal expansion of the printed circuit board to which the integrated circuit

4 package is capable of being coupled with and greater than a coefficient of thermal expansion of
5 the silicon die.

1 83. (New) An integrated circuit package comprising:
2 a silicon die having a first thickness;
3 a metallized polymer layer having a first side and a second side;
4 a transition medium having a second thickness and disposed between the silicon
5 die and the first side of the metallized polymer layer; and
6 a mold cap which encapsulates the silicon die and the transition medium, wherein
7 the mold cap and transition medium expand and contract in response to temperature changes
8 such that the die remains relatively motionless within the integrated circuit package during
9 thermal cycling.

1 84. (New) The integrated circuit package of claim 83, wherein the
2 mold cap defines a third thickness and the metallized polymer layer defines a fourth thickness,
3 wherein the third thickness and fourth thickness define a package thickness, and wherein the
4 silicon die is disposed near the middle of the package thickness so as to reduce warping of the
5 integrated circuit package in response to thermal expansion of the die.

1 85. (New) The integrated circuit package of claim 83, wherein the first
2 thickness is less than the second thickness.

1 86. (New) The integrated circuit package of claim 83, wherein the
2 mold cap and the transition medium each comprise a first mold compound, such that coefficients
3 of thermal expansion of the transition medium and mold cap are approximately equal.

1 87. (New) The integrated circuit package of claim 83, wherein the
2 mold cap and transition medium have coefficients of thermal expansion between approximately
3 $7 \times 10^{-6}/^{\circ}\text{C}$ and $15 \times 10^{-6}/^{\circ}\text{C}$.

1 88. (New) The integrated circuit package of claim 83, wherein a first
2 edge of the transition medium is coincident with a first edge of the silicon die, and a second edge
3 of the transition medium is coincident with a second edge of the silicon die.

1 89. (New) The integrated circuit of claim 83, wherein the metallized
2 polymer layer is a tape carrier comprising solder balls mounted to the second side of the
3 metallized polymer layer, the solder balls electrically contacting an etched circuit in a conductive
4 layer of the tape carrier and adapted to electrically connect the integrated circuit package to a
5 printed circuit board.

1 90. (New) The integrated circuit of claim 89, wherein the transition
2 medium and the mold cap have coefficients of thermal expansion less than a coefficient of
3 thermal expansion of the printed circuit board to which the integrated circuit package is capable
4 of being coupled with and greater than a coefficient of thermal expansion of the silicon die.